Format: Half-day (2-hours) in the (USA) morning.

Title and abstract: a concise description of the area(s) and the targeted audience.
Title: Ultra-Low-Power and highly-scalable IC: towards energy-autonomous and low-cost systems for distributed sensing

Abstract
The vision of a world where pervasive integrated electronic systems embedded in everyday life objects (e.g. household appliances, surveillance cameras, healthcare systems) are fully interconnected to collect process, and exchange useful information requires energy-autonomous systems for distributed sensing and data acquisition.
The low-cost requirement demands a small area, low design effort, digital-like shrinkage across CMOS generations, and design/technology portability. The possibility to exploit the digital (automated) design flow even for analog building blocks can dramatically reduce the design effort of any system-on-chip that faces the analog signal. Since data processing is digital but most signals from the real-world are analog, almost any electronic device that interfaces with the surrounding environment will benefit from the outcomes of this investigation. In this framework, the tutorial illustrates the concepts and the design flows which enable the implementation of analog functions by true digital circuits

Motivation:
Why is this subject timely and relevant for the 2021 MWSCAS?
The 2021 Symposium MWSCAS theme regarding also autonomous circuits and systems. A method to enable these through novel fully synthesizable ICs solutions will be described. The approach is based on making their design suitable to nanoscale IC technologies in near-threshold and voltage/energy/technology scalability [1].

What audience is expected?
The tutorial is suitable to anyone familiar with the analog building block principle and operation. The tutorial is expected to give the audience the basic understanding and methodological tools to apply a similar approach to different analog signal processing applications.

What will the participants learn?
The participant will learn how to implement ultra-low-power, compact, highly-scalable IC analog building block fully exploiting the digital design tool. This approach leads to IC designs that are natively portable across technology nodes (e.g. from 40nm to 28nm) and highly reconfigurable, thus enabling dynamic energy-quality scaling, which is critical in tightly energy-constrained application scenarios, as well as a low design effort and a fast time-to-market.

List of topics covered in the tutorial i.e., a short syllabus with the timeline.
Tentative syllabus:

- Analog – Mixed-Signal design challenges in energy-autonomous systems
- Analog physical world Versus digital processing of the information
- the Digital-Based analog differential circuit
- Fully synthesizable Analog comparator
- Fully synthesizable D/A and A/D conversion: the Dyadic Digital Pulse Modulation

- Fully synthesizable and supply voltage indifferent IC sensor: the case of a Capacitive to digital converter.

The structure and outline of the tutorial and its presentation flow.
The fully digital/synthesizable building blocks described along with the tutorial are: Wake-up oscillator, Operational Amplifier and Analog comparator, DACs and ADCs and an IC sensor (i.e. a capacitive sensor)

Wake-up oscillator.
Slow oscillators that periodically wake up the sensor nodes are fundamental building blocks in energy-autonomous sensor nodes. Being always on, wake-up oscillators' power consumption sets the very minimum power consumption of a sensor node under practical duty-cycles. The proposed oscillator can work stand-alone, with no further voltage or current reference and with a low-frequency sensitivity to the supply voltage. Thus, the actual power consumed by the always-on oscillator, and hence by the entire system is drastically reduced.

Operational Amplifiers and Analog comparator.
The state-of-the-art of fully digital/synthesizable operational amplifier is considered. The first digital-in-concept implementation of a differential pair will be discussed [3]. Then, an automatized design approach is employed to conceive analog comparison using only standard cells (logic gate) [4].

DACs
The proposed DACs significantly reduce the design effort compared to conventional analog design styles as they are based on the digital standard cells approach. Three different versions have been proposed. The first DAC with a nominal resolution of 12-bit exhibits a graceful degradation under-voltage/frequency overscaling [5]; the others are 16-bit and 12-bit versions pointing out respectively only performance and area reduction[6].

ADCs.
The first (at the best of authors-knowledge) designed and tested Current-input fully synthesizable Analog-to-Digital Converters (ADCs) will be described [7].

Capacitive sensor.
A capacitance-to-digital converter (CDC) based on swappable oscillators for low-cost systems that are directly powered by a harvester is presented. The CDC does not require any additional circuitry, suppressing any reference and voltage regulation [8].

Comparison of the performance of such circuits in terms of energy-efficiency with that of a conventional one (based on a full-custom analog approach) will be also drawn.

Reference

[1] M. Alioto (Ed.), *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, Springer, 2017
[2] **O. Aiello**, P.Crovetti, L. Lin, M. Alioto, "A pW-Power Hz-Range Oscillator Operating with a 0.3V-1.8V Unregulated Supply", *IEEE Journal of Solid-State Circuits*, Vol.54, no.5, pp.1487-1496, May 2019.
[3] P. Toledo, P.Crovetti, **O. Aiello**, M. Alioto, "Fully-Digital Rail-to-Rail OTA with Sub-1,000 µm2 Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm", *IEEE Solid State Circuits Letter*, Vol.: 3, pp: 474 - 477, 29 September 2020, doi: 10.1109/LSSC.2020.3027666
[4] **O. Aiello**, P.Crovetti, P. Toledo, M. Alioto, "Rail-to-Rail Dynamic Voltage Comparator Scalable down to pW-Range Power and 0.15V Supply", *IEEE Trans. on CAS II*, pp: 1 - 1, 12 February 2021, doi: 10.1109/TCSII.2021.3059164
[5] **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling", IEEE Transaction on Circuits and Systems I, Vol. 66, Issue 8. p. 2865- 2875, August 2019, doi:10.1109/TCSI.2019.2903464
[6] **O. Aiello**, P.Crovetti, M. Alioto, "Standard Cell-Based Ultra-Compact DACs in 40nm CMOS", IEEE Access, Vol. 7, p. 126479 - 126488, August 2019, doi: 10.1109/ACCESS.2019.2938737
[7] **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Analogue-to-Digital Converters with Minimal Design Effort Based on the Dyadic Digital Pulse Modulation", IEEE Access, Vol.: 8, Issue:1, pp: 70890-70899, Dec. 2020, doi: 10.1109/ACCESS.2020.2986949
[8] - **O. Aiello**, P. Crovetti, M. Alioto, "Capacitance-to-Digital Converter for Operation under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation", *Proc. of IEEE 2021 International Solid-State Circuits Conference (ISSCC 2021*), February 13-22, San Francisco [Virtual] doi: 10.1109/ISSCC42613.2021.9365846

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Orazio Aiello (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) from the University of Catania, Italy, in 2005 and 2008, respectively, the M.Sc degree (cum laude) from the Scuola Superiore di Catania, Italy, in 2009, and the Ph.D. degree from the Politecnico di Torino, Italy, in 2013.

From 2008 to 2009, he was an Analog IC Designer and EMC consultant for STMicroelectronics-Castelletto, Italy. In 2012, he was a Visiting Ph.D. Student with Monash University, Melbourne, Australia. In 2013, he was a Research Fellow in a joint project with FIAT-Chrysler Automobiles, Turin. In 2014, he joined NXP-Semiconductors, Nijmegen, The Netherlands, as a Mixed Signal IC Designer, and an EMC Expert. In 2015 and 2016, he was a Visiting Fellow with the University of Sydney and the University of New South Wales, Sydney, Australia.

Since 2015, he has been working with the Green IC Group, ECE Dpt., National University of Singapore, where he has also been a Marie Skłodowska-Curie Individual and Global Fellow leading the ULPIoT project funded by the European Commission.

His main research interests are focused on energy-efficient analog-mixed signal circuits and sensor interfaces.

He serves as a reviewer for several IEEE journals. He is member of the IEEE CASS Microlearning AdHoc Committee and he is/was a Technical Program Committee Member in a number of conferences such as NORCAS and APCCAS.